Nordcad Seminars

Stockholm - Copenhagen

Nordcad

Registration is free, but binding

If you fail to attend the seminar without notifying Nordcad in advance, a no-show fee of 800 DKK will be charged.

What's going to happen?

On October 8th and 9th, Nordcad invites you to two free one-day seminars in Stockholm and Copenhagen. The events showcase the latest innovations in Allegro X and OrCAD X, Release 25.1.

This is the agenda overview*. The agenda will be the same in both Stockholm and Copenhagen.

** Keep in mind that the agenda may be subject to changes.*

Joint agenda (from 08:30 to 11:00)

From 08.30 to 11.00, we will have a joint agenda. After that, you're able to go out on tracks, of which you can pick and choose as you please.

Time:	Description:
08:30	Warm welcome and light breakfast
09:00	General introduction
09:10	Cadence pitch (Vision, Flow) *Presented by Mark Hepburn, Director Product Management at Cadence.*
10:00	Break

10:15	Bringing Electronic design to the next level with Cadence AI and Allegro X AI. Presentation and live demo of Allegro X AI. *Presented by Mark Hepburn, Director Product Management at Cadence, and Ole Ejlersen, CTO at Nordcad.*
11:00	Break / End of joint agenda

Agenda for tracks #1 and #2 (from 11:15 to 16:00)

Time:	Track #1	Track #2
11:15	Get all the benefits of designing with OrCAD X Layout and its new, modern, easy-to-use capabilities. This includes revolutionary capabilities for analysis embedded within the PCB design and wizard-driven constraint management. Session includes learning how to become more efficient using the new 25.1 OrCAD PCB functionalities. *Presented by Morten Rovsing, AE at Nordcad, and Ole Ejlersen, CTO at Nordcad*	System Capture – why and how, ease of use, team design, audit, PFM, version on save, variants, and modules/reuse. Schematic design is evolving into a strategic, team-driven platform. With Allegro X System Capture, teams gain integrated analysis, real-time collaboration, shift-left workflows, and intuitive tools like version-on-save, part management, and PFM integration. This session shows how modern schematic tools enable first-pass success through simplicity and smart collaboration. *Presented by Aditya Chandra, Product Engineering Architect at Cadence*
12:00	Lunch break	

13:00	Learn how to benefit from the latest technologies in OrCAD X: • Reusing and Creating Components from existing records • Collaborative component authoring • Collaborative Design authoring with review and markup • Enhanced Find and Replace • Improve schematic documentation by aligning all settings, texts, etc. • Speed up and automate communication with review and markup on schematic and PCB designs across teams and locations. *Presented by Nitin Thapliyal, Principal Product Engineer at Cadence*	In-Design Analysis integrated with System Capture, MTBF, Thermal, etc. Unlock the full potential of your design process with Allegro X System Capture's advanced technology. This session showcases how Integrated System Capture seamlessly combines design and analysis—enabling real-time audit, stress evaluation, MTBF calculations, and integrated RF/antenna design. Learn how these capabilities drive smarter decisions, reduce risk, and accelerate time to market. *Presented by Aditya Chandra, Product Engineering Architect at Cadence*
13:45	Break	

14:00	New OrCAD X and PSpice capabilities: • Learn to easily evaluate and compare simulation results from different manufacturers. • See how many new model types will help do even more analysis than before. • Benefit from new advanced modelling capabilities, including nonlinear passives (including HF 24.1 news) *Presented by Nitin Thapliyal, Principal Product Engineer at Cadence*	Allegro X Engineering Cockpit (Schematic and Layout Editor in a single environment) • Introducing a complete PCB layout solution integrated into Schematic • Review the new, modern, intuitive interface to perform Placement, Routing, and Analysis, including export to Manufacturing. • Manage design constraints visually and hierarchically inside a docked Constraint Panel • Generate fabrication and assembly documentation quickly and easily using LiveDoc. *Presented by Mike Catrambone, Product Engineering Architect at Cadence*
14:45	Break	

15:15	Real-life example: Circuit simulation and PCB-flow: • Design Authoring using ODBC CIS part library database • Variant creation from core design • Simulation Analysis • Create a testbench to simulate a portion of a design • Simulate complete design • Advanced analysis (Optional, if time permits) • PCB generation with 3D View • Checking the supply chain information of Design using Live BOM *Presented by Nitin Thapliyal, Principal Product Engineer at Cadence*	Latest and greatest of Allegro X and OrCAD X. OrCAD and Allegro PCB Design are packed with excellent functionality to accomplish any PCB task. With version 25.1, the capabilities are significantly enhanced, incorporating several top customer requests and new functions that improve efficiency while providing ease of use. *Presented by Mike Catrambone, Product Engineering Architect at Cadence*
16:00	End of the day	

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About the presenters

Michael Catrambone:

He is the Product Engineering Architect for Allegro PCB products at Cadence Design Systems, with a focus on Allegro Core Functionality, including Constraint Management, high-speed interfaces and interconnect, and Emerging Technologies.

Mike joined Cadence in 2012 as a Principal Product Validation Engineer before moving to his current role in 2015. Before joining Cadence, he had over twenty-four years of experience in PCB development, Library Management, EDA software support, and value-added process improvement.

He is deeply involved in the Cadence user community, former Chairman of CadenceLive – Cadence User Group, and former Board Member of the International Cadence Users Group.

Mark Hepburn

He is responsible for the Cadence Allegro X Platform, with a focus on establishing a fully integrated experience for electronic system design.

Before joining Cadence, Mark served as Director of Product Management at Altium. Before joining Altium, Mark was co-founder of Perception Software, a solution provider that linked PLM to EDA.

With over 30 years of experience in EDA, Mark has held various Product Management and Application Engineering positions at Mentor Graphics, Innoveda, and Viewlogic Systems, delivering solutions for system-level performance modeling, PCB design, simulation, IP reuse, and Silicon IP.

Nitin Thapliyal

He serves as a Principal Product Engineer in the OrCAD and PSpice product group at Cadence, bringing over 14 years of expertise in the Electronic Design Automation (EDA) industry. His work primarily centers on PSpice simulation and OrCAD Capture capabilities, with a strong emphasis on CIS integration, cloud-based data management, supply chain management, and workflow automation.

Throughout his tenure at Cadence, Nitin has played a pivotal role in developing advanced simulation models for PSpice and IBIS/AMI models, specifically tailored for high-speed SerDes IP. His comprehensive experience spans PCB design flows, Spice-based circuit simulation, and Signal Integrity analysis.

Aditya Chandra

He is the Customer Engagement Architect for Allegro X products at Cadence Design Systems, specializing in Allegro X System Capture—including Constraint Management—and Allegro X Pulse. He began his journey at Cadence in 2000 as a Software Engineer and transitioned to his current role in 2005. With deep expertise in design intent capture, library development, data management, and tool extensibility through scripting, Aditya plays a pivotal role in helping customers maximize the value of their design environments.